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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,592	10/22/2003	Genichi Tanaka	027260-679	6371

21839 7590 07/22/2005

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EXAMINER

LEE, CHUN KUAN

ART UNIT	PAPER NUMBER
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2182

DATE MAILED: 07/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

87

## Office Action Summary

Application No.

10/689,592

Applicant(s)

TANAKA, GENICHI

Examiner

Chun-Kuan (Mike) Lee

Art Unit

2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07/20/2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☒ Claim(s) 14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☒ Certified copies of the priority documents have been received in Application No. 2003-115940.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 10/22/2003.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Objections*

1. Claim 14 is objected to because of the following informalities: It appears to be a duplicate of claim 1. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 are rejected under 35 U.S.C. 102(a) as being anticipated by the Synopsys design compiler tools.
3. As per claim 1, in operating the Synopsys design compiler tools within an apparatus which comprises of computational device such as a computer, workstation or server, said apparatus then have the ability to generate timing information of a functional block, comprising of the following functions:

identify intra-block input stage sequential circuits and intra-block output stage sequential circuits by comparing logical connection information with a library in which cells used for designing the functional block are registered, said intra-block input stage sequential circuits being placed in the functional block and contributing to information exchange with extra-block input stage sequential circuits outside said functional block through input pins, said intra-block output stage sequential circuits being placed in the functional block and contributing to information exchange with extra-block output stage sequential circuits outside said functional block through output pins, and the logical connection information describing connection relationships between circuit components

Art Unit: 2182

constituting the functional block, between the circuit components and the input pins and between the circuit components and the output pins;

calculate delay timing comprising of first delay times from the input pins to the intra-block input stage sequential circuits in accordance with timing constraint

information describing timing constraint on said functional block, and second delay times from said intra-block output stage sequential circuits to said output pins; and

output timing information including the first delay times and the second delay times.

4. As per claims 2-14, please see claim 1 in view of Synopsys design compiler tools operating within an apparatus.

Regarding the reference to the Synopsys design compiler tools website, please note to view the following links on the figure of design compiler family to further understand the rejections:

- Timing Optimization
- Datapath Optimization
- Power Optimization.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571)272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Popovici Dov can be reached on (571)272-4083. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3718. Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Mailed responses to this action should be sent to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231.

Faxes for Official/formal (After Final) communications or for informal or draft communications (please label "PROPOSED" or "DRAFT") sent to:

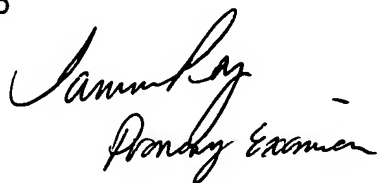
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Hand-delivered responses should be brought to:

USTPO, 2011 South Clark Place, Customer Window

Crystal Plaza Two, Lobby Room 1B03, Arlington, VA, 22202Crystal Park II, 2121.

C.K.L.  
07/20/2005

  
Donald Easman